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10/757,588	01/15/2004	Hajime Akimoto	HITA.0488	4908

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,588	AKIMOTO ET AL.	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) *9,13,25 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 18-19 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because the phrase, "provided with illuminating state controlling state" in line 5 is incorrect grammatically. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claim 9 is objected to because of the following informalities: the preamble of claim 9 does not correspond to claim 2, which claim 9 is dependent upon. Appropriate correction is required.

4. Claim 13 is objected to because of the following informalities: the phrase, "of **a** electro-luminescent element" on line 6-7 is incorrect grammatically. Additionally, the labeling of a "third switch" in the claim is seen as misleading. It appears as if there is a connection between claim 2 and claim 13 when there is none. Labeling the switch in

claim 13 as "a first switch" or even simply as "a switch" would be appropriate, and help clarify the invention. Appropriate correction is required.

5. Claim 25 is objected to because of the following informalities: claim 25 states that the device controls the "illuminating state or not-illuminating state for **each** display part." This wording is numerically inconsistent with the previously stated limitations that "**a** display part configured of a plurality of pixels" be included in the device. It seems clear that the Applicant intended the device to control the illumination state of each pixel. Appropriate correction is required.

6. Claim 27 is objected to because of the following informalities: line 3 reads "said/not-illuminating state." This wording is grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 5, 8, 10, 16, 19 and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

With respect to claims 5, 8, 16 and 19, each claim contains the limitation that a capacitor is configured as either an n-channel or p-channel MOS capacitor. This limitation was not found anywhere within the specification by the Examiner.

With respect to claims 10 and 21, each claim discusses the forming of signal lines by processing a metallic wiring layer. The Examiner was unable to locate any mention of a metallic wiring layer within the specification.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Akimoto et al. (US 2003/0067424).

With respect to claim 25, Akimoto discloses, an image display device (fig. 1) comprising:

a pixel having an electro-luminescent element (7 in fig. 1) driven to illuminate according to a display signal voltage (digital image data in fig. 9);

a display part configured of a plurality of pixels (clear from fig. 1);

a signal line used to write said display signal voltage in said pixel (17 in fig. 1);

a pixel selector (22, 32 in fig. 1) for selecting a pixel from said plurality of pixels to write said display signal voltage therein through said signal line (para. 47); and

a display signal voltage generator (21 in fig. 1) for generating is a display signal voltage;

wherein said device further comprise:

an illuminating state controller (9 in fig. 1; also see the abstract) for controlling selection of said illuminating state or non-illuminating state for each display part in which a display signal voltage is written at a time; and

a triangular wave voltage supply (27 in fig. 1) for supplying a triangular wave voltage to each of said plurality of pixels through said signal line when said illuminating state is selected for said selected pixel (see triangular wave voltage in fig. 3);

wherein one end of said electro-luminescent element provided in each pixel is connected to a common power supply (common terminal connected to the bottom of the element; also see para. 51) while the other end of said electro-luminescent element is connected to a drain electrode of an electro-luminescent element driving transistor (4 in fig. 1); and

a source electrode of said electro-luminescent element driving transistor connected to a power supply line (18 in fig. 1; para. 43), the gate of said electro-luminescent element driving transistor is connected to a drain electrode of said electro-luminescent element driving transistor through a switch (5 in fig. 1), and the gate of said electro-luminescent element driving transistor is connected to said signal line corresponding to each pixel through a connection capacitor (2 in fig. 1).

With respect to claim 26, Akimoto discloses, the image display device according to claim 25 (see above);

wherein said triangular wave voltage consists of one triangular wave (clear from fig. 3).

With respect to claim 27, Akimoto discloses, the image display device according to claim 25 (see above);

wherein selection of said illuminating state or said/not-illuminating state is repeated in each frame period (clear from fig. 21).

11. Claim 28 is rejected under 35 U.S.C. 102(e) as being anticipated by Akimoto et al. (US 2003/0214493).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 28, Akimoto discloses, a pixel display device (fig. 1) comprising:

a pixel circuit (1-5 in fig. 1) connected to a signal line (7 in fig. 1) and a power source line (8 in fig. 1);

wherein the pixel circuit comprises:

a capacitor (1 in fig. 1) directly connected to the signal line;

a driving transistor (2 in fig. 1) connected to the capacitor wherein a node is located between the driving transistor and the capacitor;

a reset switch transistor (3 in fig. 1) connected to the node at one end and connected to a drain electrode of the driving transistor at the other end;

the power source line connected to the source electrode of the driving transistor (para. 54);

an OLED transistor switch (5 in fig. 1) also connected to the drain electrode of the driving transistor at one end and connected to an organic electro-luminescent element at its other end;

a signal voltage applied to said signal line (para. 60);

a threshold voltage applied to the node and to a gate of the driving transistor (para 60); and

wherein the pixel circuit structure drives the organic electro-luminescent element with a driving current of the driving transistor free from an influence from threshold voltage variation (para. 82).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-4, 6-7, 9, 12-15, 17-18, 20 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Stewart (US 5,302,966).

With respect to claim 1, Akimoto discloses, an image display device (fig. 1), comprising:

a pixel having an electro-luminescent element (7 in fig. 1) driven to illuminate according to a display signal voltage;

a display part configured by a plurality of pixels (clear from fig. 1);

a signal line (7 in fig. 1) used to write said display signal voltage in said pixel (see write period in fig. 2);

a pixel selector (22 in fig. 1) for selecting a pixel from said plurality of pixels so as to write said display signal voltage therein through said signal line; and

a display signal voltage generator (21 in fig. 1) for generating said display signal voltage;

wherein said display device further includes;

an illuminating state controller (32, 9 in fig. 1) for controlling a selection of illuminating state or non-illuminating state for each of said plurality of pixels at a time.

Akimoto further discloses, a constant voltage supply, as evidenced by the signal line data during the write period in figure three. During an illumination period, Akimoto supplies a triangular signal amplitude as seen in figure three.

Akimoto does not expressly disclose supplying a constant voltage to each pixel during the illuminating state.

Stewart discloses, an image display device having an electro-luminescent element pixel circuit (42 in fig. 2a), wherein a constant voltage supply (64, 62 in fig. 2a) provides a constant voltage to the pixel through a signal line (48 in fig. 2a) when said illuminating state is selected for said selected pixel (col. 3, lines 32-34).

Stewart and Akimoto are analogous art because they are both from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the triangular signal amplitude of Akimoto with the constant hold voltage of Stewart.

The motivation for doing so would have been to attain different visual characteristics (Akimoto; end of para. 48).

Therefore it would have been obvious to combine Akimoto with Stewart for the benefit of different visual characteristics to obtain the invention as specified in claim 1.

With respect to claim 2, Akimoto and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein one end of said electro-luminescent element provided in each pixel is connected to a common power supply (common terminal connected to the element in fig. 1; also see end of para. 51) while the other end of said electro-luminescent element is connected to a first source/drain electrode of an electro-luminescent element driving transistor (4 in fig. 1) through a first switch (9 in fig. 1) and,

a second source/drain electrode of said electro-luminescent element driving transistor is connected to a power supply line (18 in fig. 1; para. 43),

and the gate of said electro-luminescent element driving transistor (4 in fig. 1) is connected to a first source/drain electrode of said electro-luminescent element driving transistor through a second switch (5 in fig. 1), and

the gate of said electro-luminescent element driving transistor is connected to said signal line corresponding to each pixel through a connection capacitor (2 in fig. 1).

With respect to claim 3, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein said first source/drain electrode is a drain electrode and said second source/drain electrode is a source electrode (para. 43).

With respect to claim 4, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein each of said first switch, said second switch, and said electro-luminescent element driving transistor is a p-channel transistor (fig. 4; also see para. 62).

With respect to claim 6, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein each of said first switch, said second switch, and said electro-luminescent element driving transistor is a polycrystalline silicon thin film transistor (para. 43).

With respect to claim 7, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein each of said first switch, said second switch, and said electro-luminescent element driving transistor is an n-channel transistor (fig. 6; also see para. 69).

With respect to claim 9, Akimoto and Stewart disclose, the display device according to claim 2 (see above).

Stewart further discloses, the use of amorphous silicon thin film transistors (col. 7, line 67 – col. 8, line 5).

It is well known in the art that amorphous silicon thin film transistors are more uniform over large areas than polycrystalline silicon thin film transistors.

With respect to claim 12, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein said electro-luminescent element driving transistor is actually driving in a sub-threshold area in which its gate-source voltage is a threshold voltage and under (para. 47).

With respect to claim 13, Akimoto and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein one end of said electro-luminescent element provided in each pixel is connected to a common power supply (common terminal connected to the element in fig. 1; also see para. 51);

and the other end of said electro-luminescent element is connected to a first source/drain electrode of an electro-luminescent element driving transistor (4 in fig. 1; the element is still considered connected to the driving transistor even if the connection travels through transistor, 9) and,

a second source/drain electrode of said electro-luminescent element driving transistor is connected to a power supply line (18 in fig. 1; para. 43),

and the gate of said electro-luminescent element driving transistor (4 in fig. 1) is connected to a first source/drain electrode of said electro-luminescent element driving transistor through a third switch (5 in fig. 1), and

the gate of said electro-luminescent element driving transistor is connected to said signal line corresponding to each pixel through a connection capacitor (2 in fig. 1).

With respect to claims 14-15, 17-18, 20 and 23, as these claims are identical to previously rejected claims 3-4, 6-7, 9 and 12, respectively, these claims are rejected on the same merits shown above.

With respect to claim 24, Akimoto and Stewart disclose, the image display device according to claim 1 (see above).

Akimoto further discloses, wherein selection of said illuminating/non-illuminating state is repeated in each frame period (clear from fig. 21, that the operation repeats indefinitely).

14. Claims 5, 8, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Stewart (US 5,302,966) and further in view of Misawa et al. (US 5,250,931).

With respect to claim 5, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein each of said first switch, said second switch, and said electro-luminescent element driving transistor is configured as a p-channel transistor (see fig. 4; para. 62).

Neither Akimoto nor Stewart expressly disclose, that said connection capacitor is a MOS capacitor that uses a p-channel.

Misawa discloses, a pixel capacitor (305 in fig. 15a/b) that is a p-channel MOS capacitor (col. 14, lines 61-68).

Misawa, Akimoto and Stewart are analogous art because they are all from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the MOS capacitors taught by Misawa in the display device of Akimoto and Stewart.

The motivation for doing so would have been to lower the number of manufacturing steps to form the display device (Misawa; col. 14, lines 55-60).

Therefore it would have been obvious to combine Misawa with Akimoto and Stewart for the benefit of simplified manufacturing to obtain the invention as specified in claim 5.

With respect to claim 8, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein each of said first switch, second switch, and said electro-luminescent element driving transistor is an n-channel transistor (fig. 6; also see para. 69).

Neither Akimoto nor Stewart expressly disclose, that said connection capacitor is a MOS capacitor that uses an n-channel.

Misawa discloses, a pixel capacitor (305 in fig. 15a/b) that is an n-channel MOS capacitor (col. 14, lines 61-68).

Misawa, Akimoto and Stewart are analogous art because they are all from the same field of endeavor namely pixel control circuitry and driving methods for electro-luminescent display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the MOS capacitors taught by Misawa in the display device of Akimoto and Stewart.

The motivation for doing so would have been to lower the number of manufacturing steps to form the display device (Misawa; col. 14, lines 55-60).

Therefore it would have been obvious to combine Misawa with Akimoto and Stewart for the benefit of simplified manufacturing to obtain the invention as specified in claim 8.

With respect to claims 16 and 19, as these claims are identical to previously rejected claims 5 and 8, respectively, these claims are rejected on the same merits shown above.

15. Claims 10 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Stewart (US 5,302,966) and further in view of Akimoto et al. (US 6,670,936; hereinafter: Akimoto-'936).

With respect to claim 10, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Akimoto further discloses, wherein said signal line and said power supply line are disposed in parallel (clear from fig. 1 that 17 and 18 are parallel).

Neither Akimoto nor Stewart expressly disclose, forming the signal line and power supply by processing the same metallic wiring layer.

Akimoto-'936 discloses, a signal line (4 in fig. 1) and a power supply line (8 in fig. 1) are disposed in parallel (clear from fig. 1) and formed by processing the same metallic wiring layer (col. 6, line 62 – col. 7, line 7).

Akimoto, Stewart and Akimoto-'936 are all analogous art because they are all form the same field of endeavor namely, pixel control circuitry and driving methods for image display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the signal and power supply lines of Akimoto and Stewart on the same metallic wiring layer as taught by Akimoto-'936.

The motivation for doing so would have been to simplify the manufacturing process (Akimoto-'936; col. 7, lines 6-7).

Therefore it would have been obvious to combine Akimoto-'936 with Akimoto and Stewart for the benefit of a simplified manufacturing process to obtain the invention as specified in claim 10.

With respect to claim 21, as this claim is identical to previously rejected claim 10, this claim is rejected on the same merits shown above.

16. Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Stewart (US 5,302,966) and further in view of Miyajima et al. (US 6,812,912).

With respect to claim 11, Akimoto and Stewart disclose, the image display device according to claim 2 (see above).

Neither Akimoto nor Stewart expressly disclose, that the connection capacitor is provided on the signal line in layers.

Miyajima discloses providing a capacitor (30 in fig. 14) that is provided on a signal line (data line; 22 in fig. 14) in layers (clear from fig. 15; also see col. 17, lines 41-48).

Akimoto, Stewart and Miyajima are all analogous art because they are all form the same field of endeavor namely, pixel control circuitry for image display devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the connection capacitor of Akimoto and Stewart on the signal line in layers as taught by Miyajima.

The motivation for doing so would have been to increase the contrast and display quality of the image display device (Miyajima; col. 18, lines 38-39).

Therefore it would have been obvious to combine Miyajima with Akimoto and Stewart for the benefit of a higher quality display device to obtain the invention as specified in claim 11.

With respect to claim 22, as this claim is identical to previously rejected claim 11, this claim is rejected on the same merits shown above.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Wlb
10/19/06

AMR A. AWAD
SUPERVISORY PATENT EXAMINER